REMARKS

The rejection of claims 3, 4, 6-11, 13 and 14 under 35 USC 112, first paragraph, as failing to comply with the written description requirement is respectfully traversed.

The Examiner has alleged that the claims contain subject matter not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors at the time the application was filed had possession of the claimed invention. To the contrary, the claims define output signals which clearly correlate to the specification and drawings in the application.

In this regard, the first timing signal of claims 3, 4, 6-8 corresponds to the output of the counter circuit 73, whereas the second timing signal in claims 3, 4, 6-8 corresponds to the output of the counter circuit 74. In claims 6, 7 and 9, the "third counter" corresponds to the high-gate counter 90 in conjunction with the gate circuit 91 and the "fourth counter" corresponds to the low-gate counter 93 in conjunction with the gate circuit 94. In claims 10 and 13, the "third timing signal" corresponds to the output of the high-edge output circuit 99 and the "fourth timing signal" corresponds to the output of the low edge output circuit 102. In claims 11 and 14, "the fifth timing signal" corresponds to the output of the delay circuit 101 and the "sixth timing signal" corresponds to the output of the delay circuit 103.

Accordingly, the rejection of claims 3, 4, 6-11, 13 and 14 under 35 USC 112, first paragraph is clearly in error and should be withdrawn.

The rejection of claims 5 and 12 under 35 USC 112, first paragraph is also believed to be in error. However, claims 5 and 12 have been amended to overcome any misunderstanding regarding which additional features in claims 5 and 12 have been added as dependent upon claims 4 and 10 respectively.

The rejection of claims 1, 2, 16 and 17 under 35 USC 102(b) as being anticipated by Hedstrom et al (USP 5,272,448) is respectfully traversed.

Claims 1 and 17 are directed to a signal processing circuit and method in which the effects of a chattering noise component is contemplated based upon the ability to absorb and tolerate a noise component. The switching of the polarity of the input pulse signal between positive and negative occurs in a predetermined period within which a noise component may exist with the period of each of the positive and negative polarities of the input signal varied based on a predetermined number of counts of clock pulses.

Hedstrom has no corresponding teaching and does not consider the effects of a chattering noise component nor does Hedstrom teach of disclose the concept of setting the period of each polarity of the input signal based on a predetermined number of counted clock pulses.

According to the present invention, the count value of a gate counter based on the positive polarity of the input FM pulse signal and the count value of a gate counter based on the negative polarity of the input pulse signal are used to set (determine) a period for the respective positive and negative polarities of the input pulse signal. In this way, the effects of chattering noise occurring when an FM signal crosses the zero level as shown in Fig. 3 is taken into consideration. That is, a predetermined period of each of the positive and negative polarities of the input pulse signal, throughout which period a corresponding one of the counters cumulatively counts the clock pulses, is determined based on the count value of the other one of the counters. For instance, referring to Fig. 8, when the count value of the counter circuit 73 indicated by (e) reaches a certain value represented by a period Tc at time t3, the count value of the counter circuit 74 indicated by (f) is reset (cleared) after a certain delay. Based on this, the period of the negative polarity of the input pulse signal is determined. Thereafter, when the count value of the counter circuit 74 reaches the certain value at time t6, the count value of the counter circuit 73 is reset (cleared) after a certain delay. In the same fashion, a period of the positive polarity of the input pulse signal is determined. Thus, the period of both of the positive and negative polarities of the input pulse signal can be determined, taking a period of chattering (for instance, t1-t2 or t4-t5) into consideration. As a result, a chattering noise component can be absorbed.

On the other hand, Hedstrom which teaches an FM signal demodulation technique that reduces noise generation in demodulating and transmitting a received FM signal, neither acknowledges nor suggests how to eliminate or absorb a chattering noise component included in an input pulse signal, and thereby control the generation of noise in a resultant digital signal obtained based on the input pulse signal.

Referring to Fig. 1 of Hedstrom, two counters 22 and 24 are disclosed for counting clock pulses. However, the count value of each one of the counters 22 and 24 is cleared every time the polarity of the FM IF signal 26 is switched. The period of each polarity of the input FM IF signal 26 is determined as the polarity of the signal 26 is switched between positive and negative. However, no count value of either the counter 22 or the counter 24 is made to determine the period of each polarity of the signal 26. Thus, according to Hedstrom, it is impossible to absorb a chattering noise component included in the signal 26 because during a period of chattering as indicated by, for instance, t1-t2 in Fig. 8 of the present application, a corresponding one of the counters 22 or 24 would output a count value and be cleared every time the polarity of the input FM pulse signal indicated by (a) in Fig. 8 is switched. The configuration of Hedstrom is basically equivalent to the technique described in the PRIOR ART section in the specification of the present application, in which a chattering component cannot be eliminated, so that an accurate digital signal cannot be obtained.

For all of the above reasons, claims 1 and 17 are clearly patentable over Hedstrom either under 35 USC 102 or under 35 USC 103.

Claims 2 and 16 are dependent claims which depend from claim 1 and are therefore believed patentable for the same reasons as given above.

New claims 18-23 relate to the feature of the present invention described in the third embodiment with reference to Figs. 11 and 12. The third embodiment discloses a technique of generating a phase difference pulse signal having a predetermined phase difference with respect to an input pulse signal and determining the counter output timing based on a pulse edge of the phase difference pulse signal.

Reconsideration and allowance of claims 1-12 and 15-17 and the new claims 18-23, is respectfully solicited.

Respectfully submitted,

Eugene Lieberstein
Reg, No. 24,645

MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed: Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313 on June 23, 2004.

Dated: June 23, 2004 Signed:

AMENDMENT TO CLAIMS

--1. (Currently Amended) A signal processing circuit generating a digital signal based on an input pulse signal, the signal processing circuit comprising:

a clock pulse output ~~circuit which~~ part configured to ~~outputs~~ output clock pulses ~~having one of positive and negative polarities~~ in accordance with a polarity of the input pulse signal ~~for~~ in a predetermined period ~~which includes~~ including a pulse of the input pulse signal and tolerating a noise component, the polarity of the input pulse signal being switchable between positive and negative in the predetermined period;

a counter ~~circuit which~~ part configured to ~~counts~~ count the clock pulses output when the polarity of the input pulse signal is positive and the clock pulses output when the polarity of the input pulse signal is negative independent of each other;

a setting part configured to set the predetermined period based on a predetermined counted value of the counter part; and

an output ~~circuit which~~ part configured to ~~outputs~~ output the digital signal based on a counted value of said counter ~~circuit~~ part.

2. (Currently Amended) The signal processing circuit as claimed in claim 1, wherein:

said clock pulse output ~~circuit~~ part comprises:

a first clock pulse output ~~circuit which~~ part configured to ~~outputs~~ output the clock pulses when the polarity of the input pulse signal ~~has a~~ is positive ~~polarity~~; and

a second clock pulse output ~~circuit which~~ part configured to ~~outputs~~ output the clock pulses when the polarity of the input pulse signal ~~has a~~ is negative ~~polarity~~; and

said counter ~~circuit~~ part comprises:

a first counter ~~circuit which~~ part configured to ~~counts~~ count the clock pulses supplied from said first clock pulse output ~~circuit~~ part; and

a second counter ~~circuit which~~ part configured to ~~counts~~ count the clock pulses supplied from said second clock pulse output ~~circuit~~ part.

3. (Currently Amended) The signal processing circuit as claimed in claim 2, wherein:

said first counter ~~circuit~~ part outputs a first timing signal at ~~a first~~ the predetermined counted value;

said second counter ~~circuit~~ part outputs a second timing signal at ~~a second~~ the predetermined counted value; and

said output ~~circuit~~ part comprises:

a first latch ~~circuit which~~ part configured to ~~latches~~ latch a counted value of said first counter

~~circuit~~ part based on the second timing signal; and

a second latch ~~circuit which~~ part configured to ~~latches~~ latch a counted value of said second counter ~~circuit~~ part based on the first timing signal.

4. (Currently Amended) The signal processing circuit as claimed in claim 3, wherein:

said output ~~circuit~~ part comprises:

a first delay ~~circuit which~~ part configured to ~~delays~~ delay the first timing signal; and

a second delay ~~circuit which~~ part configured to ~~delays~~ delay the second timing signal;

said first counter ~~circuit~~ part is reset by an output signal of said second delay ~~circuit~~ part; and

said second counter ~~circuit~~ part is reset by an output signal of said first delay ~~circuit~~ part.

5. (Currently Amended) The signal processing circuit as claimed in claim 4, wherein said output ~~circuit~~ part further comprises:

a flip flop ~~which is~~ set by the output signal of said first delay ~~circuit~~ part and ~~is~~ reset by the output signal of said second delay ~~circuit~~ part; and

a switching ~~circuit which~~ part configured to ~~switches~~ switch, based on an output of said flip flop, an output thereof between ~~outputs of~~ the counted values latched by said first and second latch ~~circuits~~ parts, respectively.

6. (Currently Amended) The signal processing circuit as claimed in claim 2, wherein said counter ~~circuit~~ part further comprises:

a third counter ~~circuit which~~ part configured to ~~counts~~ count the clock pulses supplied from said first clock pulse output ~~circuit~~ part; and

a fourth counter ~~circuit which~~ part configured to ~~counts~~ count the clock pulses supplied from said second clock pulse output ~~circuit~~ part~~; and~~,

~~a~~ wherein the setting ~~circuit which~~ part sets the predetermined period based on respective predetermined counted values of said third and fourth counter ~~circuits~~ parts.

7. (Currently Amended) The signal processing circuit as claimed in claim 6, wherein:

said third counter ~~circuit~~ part outputs a first timing signal at the predetermined counted value of said third counter ~~circuit~~ part

said fourth counter ~~circuit~~ part outputs a second timing signal at the predetermined counted value of said fourth counter ~~circuit~~ part; and

said setting ~~circuit~~ part outputs, based on the first and second timing signals, a signal which determines the predetermined period.

8. (Currently Amended) The signal processing circuit as claimed in claim 7, wherein said setting ~~circuit~~ part comprises a flip flop ~~which is~~ set by the first timing signal and ~~is~~ reset by the second timing signal.

9. (Currently Amended) The signal processing circuit as claimed in claim 8, wherein one of the counted values of said third and fourth counter ~~circuits~~ parts is reset when said flip flop is reset.

10. (Once Amended) The signal processing circuit as claimed in claim 8, wherein said output ~~circuit~~ part comprises:

a rising edge output ~~circuit which~~ part configured to ~~outputs~~ output a third timing signal at a rising edge of an output of said flip flop;

a falling edge output ~~circuit which~~ part configured to ~~outputs~~ output a fourth timing signal at a falling edge of the output of said flip flop;

a first latch ~~circuit which~~ part configured to ~~latches~~ latch a counted value of said first counter ~~circuit~~ part based on the fourth timing signal; and

a second latch ~~circuit which~~ part configured to ~~latches~~ latch a counted value of said second counter ~~circuit~~ part based on the third timing signal.

11. (Currently Amended) The signal processing circuit as claimed in claim 10, wherein:

said output ~~circuit~~ part further comprises:

a first delay ~~circuit which~~ part configured to ~~delays~~ delay the third timing signal and ~~outputs~~ output a fifth timing signal; and

a second delay ~~circuit which~~ part configured to ~~delays~~ delay the fourth timing signal and ~~outputs~~ output a sixth timing signal;

said first counter ~~circuit~~ part is reset by the sixth timing signal; and

said second counter ~~circuit~~ part is reset by the fifth timing signal.

12. (Currently Amended) The signal processing circuit as claimed in claim 10, wherein said output ~~circuit~~ part further comprises a switching ~~circuit which~~ part configured to ~~switches~~ switch, based on an output of said flip flop, an output thereof between ~~outputs of~~ the counted values latched by said first and second latch ~~circuits~~ parts, respectively.

16. (Once Amended) The signal processing circuit as claimed in claim 1, wherein said output ~~circuit~~ part includes a digital low-pass filter.

17. (Once Amended) A method of generating a digital signal based on an input pulse signal, the method comprising the steps of:

(a) outputting clock pulses ~~having one of positive and negative polarities~~ in accordance with a polarity of the input pulse signal ~~for~~ in a predetermined period including a pulse of the input pulse signal and tolerating a noise component, the polarity of the input pulse signal being switchable between positive and negative in the predetermined period;

(b) counting the clock pulses output when the polarity of the input pulse signal is positive and the clock pulses output when the polarity of the input pulse signal is negative independent of each other;

(c) setting the predetermined period based on a predetermined counted value of the counter part; and

~~(c)~~ (d) outputting the digital signal based on ~~the~~ a counted value obtained in said step (b).

18. (New) A signal processing circuit generating a digital signal based on an input pulse signal, the signal processing circuit comprising:

a clock pulse output part configured to output clock pulses in accordance with a polarity of the input pulse signal in a predetermined period including a pulse of the input pulse signal and tolerating a noise component, the polarity of the input pulse signal being switchable between positive and negative in the predetermined period;

a counter part configured to count the clock pulses output when the polarity of the input pulse signal is positive and the clock pulses output when the polarity of the input pulse signal is negative independent of each other;

a setting part configured to set the predetermined period based on a phase difference pulse signal having a predetermined phase difference with respect to the input pulse signal; and

an output part configured to output the digital signal based on a count value of the counter part.

19. (New) The signal processing circuit as claimed in claim 18, wherein:

the clock pulse output part includes:

a first clock pulse output part configured to output the clock pulses when the polarity of the input pulse signal is positive; and

a second clock pulse output part configured to output the clock pulses when the polarity of the input pulse signal is negative; and

the counter part includes:

a first counter part configured to count the clock pulses supplied from the first clock pulse output part; and

a second counter part configured to count the clock pulses supplied from the second clock pulse output part.

20. (New) The signal processing circuit as claimed in claim 19, wherein:

the setting part includes:

a rising edge output part configured to output a first timing signal at a rising edge of the phase difference pulse signal; and

a falling edge output part configured to output a second timing signal at a falling edge of the phase difference pulse signal; and

the output part includes:

a first latch part configured to latch a count value of the first counter part based on the first timing signal; and

a second latch part configured to latch a count value of the second counter part based on the second timing signal.

21. (New) The signal processing circuit as claimed in claim 20, wherein:

the output part includes:

a first delay part configured to delay the first timing signal and output a third timing signal; and

a second delay part configured to delay the second timing signal and output a fourth timing signal;

the first counter part is reset based on the third timing signal; and

the second counter part is reset based on the fourth timing signal.

22. (New) The signal processing circuit as claimed in claim 20, wherein:

the output part includes:

a third delay part configured to delay the phase difference pulse signal and output a delayed phase difference pulse signal; and

a switching part configured to switch, based on the delayed phase difference pulse signal, an output thereof between the first count value latched by the first latch part and the second count value latched by the second latch part.

23. (New) A method of generating a digital signal based on an input pulse signal, the method comprising the steps of:

(a) outputting clock pulses in accordance with a polarity of the input pulse signal in a predetermined period including a pulse of the input pulse signal and tolerating a noise component, the polarity of the input pulse signal being switchable between positive and negative in the predetermined period;

(b) counting the clock pulses output when the polarity of the input pulse signal is positive and the clock pulses output when the polarity of the input pulse signal is negative independent of each other;

(c) setting the predetermined period based on a phase difference pulse signal having a predetermined phase difference with respect to the input pulse signal; and

(d) outputting the digital signal based on a count value obtained in said step (b).

Amended SPECIFICATION, Page 17, lines 11-28.

The switching circuit 78 performs a switching operation so that the ~~positive~~ negative polarity counted value input to the A input is output when the Q output is at a high level, and the ~~negative~~ positive polarity counted value input to the B input is output when the Q output is at a low level. The output of the switching circuit 78 is shown as the output counted value of Fig. 8(1). That is, the output of the switching circuit 78 is switched to the positive polarity counted value by the carry pulse (positive) and to the negative polarity counted value by the carry pulse (negative). When these carry pulses are supplied to the OR gate 83, the output shown in Fig. 8 (m) is output from the OR gate 83. The output of the OR gate 83 is supplied to the delay circuit 82, so that the output is delayed as shown in Fig. 8 (n). The delay provided by the delay circuit 82 is determined in consideration of a period which the switching circuit 78 requires in outputting the counted value.